IN THE CLAIMS:

Please enter the following claims:

1. (currently amended) A method of performing a physical verification of the layout of an integrated circuit comprising the steps of:

identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors;

measuring parameters of each of said sub-circuits, and comparing the measured parameters of each of said sub-circuits against corresponding parameters of a schematic netlist; and

determining if all of said comparisons returns a correct correlation, and reporting when any of said comparisons returns a mismatched correlation, said comparison being performed in a sub-circuit extraction mode when said transistor is identified as a sub-circuit; otherwise, said comparison being performed in a flat extraction mode.

2. Cancelled

3. (original) The method of claim 1, wherein said transistor in said layout is a single fingered field-effect transistor (FET).

4. (original) The method of claim 1, wherein said transistor in said layout is a multi-fingered field-effect transistor (FET).

5. (original) The method of claim 4, wherein the measured parameters of said multi-fingered transistor are respectively compared to corresponding parameters of said schematic netlist.

6. (original) The method of claim 4, wherein said FET transistor comprises at least two gate regions shorted to each other, at least one drain and two source diffusion regions, said two source diffusion regions being shorted to each other, or at least one source and two drain diffusion regions, said two drain diffusion regions being shorted to each other .

7. (original) The method of claim 6, wherein said layout includes first marker shapes to identify said source or drain diffusion regions between pairs of said FET gate regions.

8. (original) The method of claim 7, wherein said layout includes second marker shapes to identify said source or drain diffusion regions occurring outside said pairs of FET gate regions.

9. (original) The method of claim 8, wherein said first and second marker shapes are used to form a netlist for said FET transistor.

10. (original) The method of claim 1, wherein said comparison of the measured parameters of each of said sub-circuits against the corresponding parameters of the schematic netlist
further comprises comparing the diffusion dimensions of the source and the drain of said transistor to said schematic netlist.

11. (currently amended) A method for creating a device layout comprising the steps of:

providing device model parameters that support an extraction of a list of device layout geometric parameters, said device model parameters comprising channel length (L), finger width (WF), number of fingers (NF), left diffusion length (DIFFL), middle diffusion length (DIFFM), and right diffusion length (DIFFR) of an FET transistor; and

providing specific marker shapes to define the device layout geometric parameters,.

12. Cancelled

13. (currently amended) The method of claim [[12]] 11, wherein a minimum set of three FET transistor marker shapes (LEFT, MULTI, and RIGHT) are used for bulk Si and SOI technologies.

14. (original) The method of claim 11, wherein said devices are selected from the group consisting of bipolar junction transistors (BJT), hetero-junction bipolar transistors (HBT), and compounded semiconductor transistors.

15. (original) The method of claim 11, wherein further marker shapes are added to non-FET devices to perform a sub-circuit based extraction.

16. (original) The method of claim 15, wherein non-FET devices are selected from the group consisting of integrated on-chip inductors, integrated on-chip capacitors, resistors, and varactors.

17. (currently amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for performing a physical verification of the layout of an integrated circuit, said method steps comprising:

identifying transistors in a sub-circuit configuration that includes respective interconnections linked to each of said transistors;

measuring parameters of each of said sub-circuits, and comparing the measured parameters of each of said sub-circuits against corresponding parameters of a schematic netlist; and

determining if all of said comparisons returns a correct correlation, and reporting when any of said comparisons returns a mismatched correlation, said comparison being performed in a sub-circuit extraction mode when said transistor is identified as a sub-circuit; otherwise, said comparison being performed in a flat extraction mode.